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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/994,023
Filing Date: November 27, 2001
Appellant(s): NIGHTINGALE, ANDREW MARK

John R. Lastova
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 28 September 2007 appealing from the Office action mailed 21 February 2001.

(1) Real Party in Interest

A statement identifying by name the real part in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellants statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief are correct.

(8) Evidence Relied Upon

(8.1) Rajsuman et al. "Method and Apparatus for SOC Design Validation", U.S. Patent No. 6,678,645, hereafter referred to as Rajsuman

(9) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

(9.1) Claim(s) 1-2, 4-12, 14-22, and 24-30 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by **Rajsuman et al. "Method and Apparatus for SOC Design Validation" U.S. Patent 6,678,645.**

Regarding Claims 1, 11, and 21

Rajsuman et al. discloses an apparatus, method, and computer program product embodied on a computer-readable medium and comprising code that when executed controls a computer for simulating data processing operations performed by a data processing apparatus, said apparatus comprising:

a hardware simulator responsive to one or more stimulus signals to generate one or more response signals simulating a response of said data processing apparatus to said one or more stimulus signals if applied to said data processing apparatus; **(Column 5, Lines 41-48)**

a plurality of signal interface controllers **(labeled as Verification Unit in Rajsuman et al.)** coupled to said hardware simulator, each signal interface controller serving to perform one or more simulation actions transferring at least one of one or more stimulus signals and one or more response signals between a corresponding portion of said hardware simulator and said signal interface controller as part of simulating said data processing operations; **(Column 5, Lines 43-44)** and

a test scenario manager coupled to said plurality of signal interface controllers and operable to transfer test scenario controlling messages to said plurality of signal interface controllers, at least one of said test scenario controlling messages including: **(Column 5, Lines 32-34)**

(i) data defining a simulation action to be performed by a signal interface controller; and **(Column 5, Lines 32-38)**

(ii) data defining when said signal interface controller should perform said simulated action. **(Column 10, Lines 25-26)**

a time generator coupled to said plurality of signal interface controllers and said test scenario manager for generating messages specifying time defining events corresponding to advancement of simulated time for said hardware simulator, **(Figure 5. Column 7, Line 49-59. Column 10, Lines 56-45. Column 11, Lines 4-11. Column 12, Lines 1-7)**

wherein said test scenario manager includes a shared data memory into which a signal interface controller may store data using a test scenario controlling message sent from said signal interface controller to said test scenario manager via said shared data memory independently of advancement of simulated time by said

messages specifying time defining events, said data being readable from said shared data memory by another signal interface controller. **(Column 7, Line 60 – Column 8 Line 5. Figure 5)**

Regarding Claims 2, 12, and 22

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 1, 11, and 21 respectively; wherein said data defining when said signal interface controller should perform said simulated action includes at least one of:

(i) a time value; **(Column 10, Lines 25-26)**

(ii) a delay value; and

(iii) a value specifying said simulated action should be performed when a specified event is simulated as occurring. **(Column 10, Lines 35-36)**

Regarding Claims 4, 14, and 24

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 1, 11, and 21 respectively; wherein a first signal interface controller is responsive to simulation results captured by a second signal interface controller, written to said shared data memory by said second signal interface controller and then read from said shared data memory by said first signal interface controller. **(Column 8, Lines 2-5, and Figure 6, Elements 671-676, 76, and 661-665)**

Regarding Claims 5, 15, and 25

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 1, 11, and 21 respectively; wherein said hardware simulation is simulated using software running upon a general purpose computer. **(Column 5, Lines 32-34)**

Regarding Claims 6, 16, and 26

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 1, 11, and 21 respectively; wherein each signal interface controller includes an action queue of simulation actions to be performed by said signal interface controller. **(Column 8, Lines 13-15)**

Regarding Claims 7, 17, and 27

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 6, 16, and 26 respectively; wherein each signal interface controller includes a test scenario manager interface operable to exchange test scenario controlling messages with said test scenario manager and to add simulation actions to said action queue. **(Column 8, Lines 6-9, and 13-15)**

Regarding Claims 8, 18, and 28

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 6, 16, and 26 respectively; wherein each signal interface controller includes a peripheral interface operable to transform simulation actions specified in said action queue into signal values exchanged with said hardware simulation. **(Column 6, Lines 62-63)**

Regarding Claims 9, 19, and 29

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 1, 11, and 21 respectively; wherein test scenario manager sends a machine generated sequence of simulation actions to said plurality of signal interface controllers to perform random simulation testing of said data processing apparatus. **(Column 2, Lines 31-32)**

Regarding Claims 10, 20 and 30

Rajsuman et al. discloses an apparatus, method, and computer program dependent on Claims 1, 11, and 21 respectively; wherein said test scenario manager is operable as a master device and said plurality of signal interface controllers are operable as slave devices to said master device. **(Column 13, Lines 7-10)**

(10) Response to Argument

Response to Argument – Prior Art Rejection

(10.1) Appellant argues that the reference does not disclose a shared data memory.

Examiners Answer:

The Examiner stated in the previous rejection "***However, as per Column 7, Line 60 - Column 8 Line 5 as well as Figure 5 the control CPU's are connected to the Main System CPU as well as each other in order to allow for data transfer, synchronization, etc. Therefore since the verification units are connected to Control CPU and the Standard Bus, there is a connection between the elements and allows communication between them for situations of arbitration, synchronization, etc.***" The VU's discussed in the reference are connected in many ways to allow for communication. In further support of this position, Column 7, Lines 49-59 states:

> As shown in FIGS. **4B** and **5**, the system contains a bus based architecture. The system bus **64** can be an industry standard bus such as VME, VXI or PCI bus that allows data transfer from the main system CPU **62** to the pins of verification units (VUs) 66_1–66_5. The system pins are configurable by the user, i.e., a user can group test pins of the validation units (VUs) according to the I/Os of silicon ICs 68_1–68_5, representing the individual cores A–E. The silicon ICs 68_1–68_5 are mounted on pin electronics and device load boards (hereafter "pin electronics") 69_1–69_5 and are connected to one another via an interconnect bus **71**.

This section shows that the VU's are connected to one another via an interconnect bus. In addition Column 10, Lines 56-45 and Column 11, Lines 4-11 state:

> (1) Use interconnect bus **71** that connects various silicon ICs **68** as shown in FIG. **5** to model the SoC on-chip bus. This is a system bus that connects various cores A–E which models the behavior of the on-chip bus. This maps instruction and data flow at an SoC level (from one core to another core) onto instruction and data flow at a design validation station level (from one VU to another VU). Hence, this bus captures any request/grant protocol of the SoC on-chip bus as well as all data transactions at each interface of the individual cores.

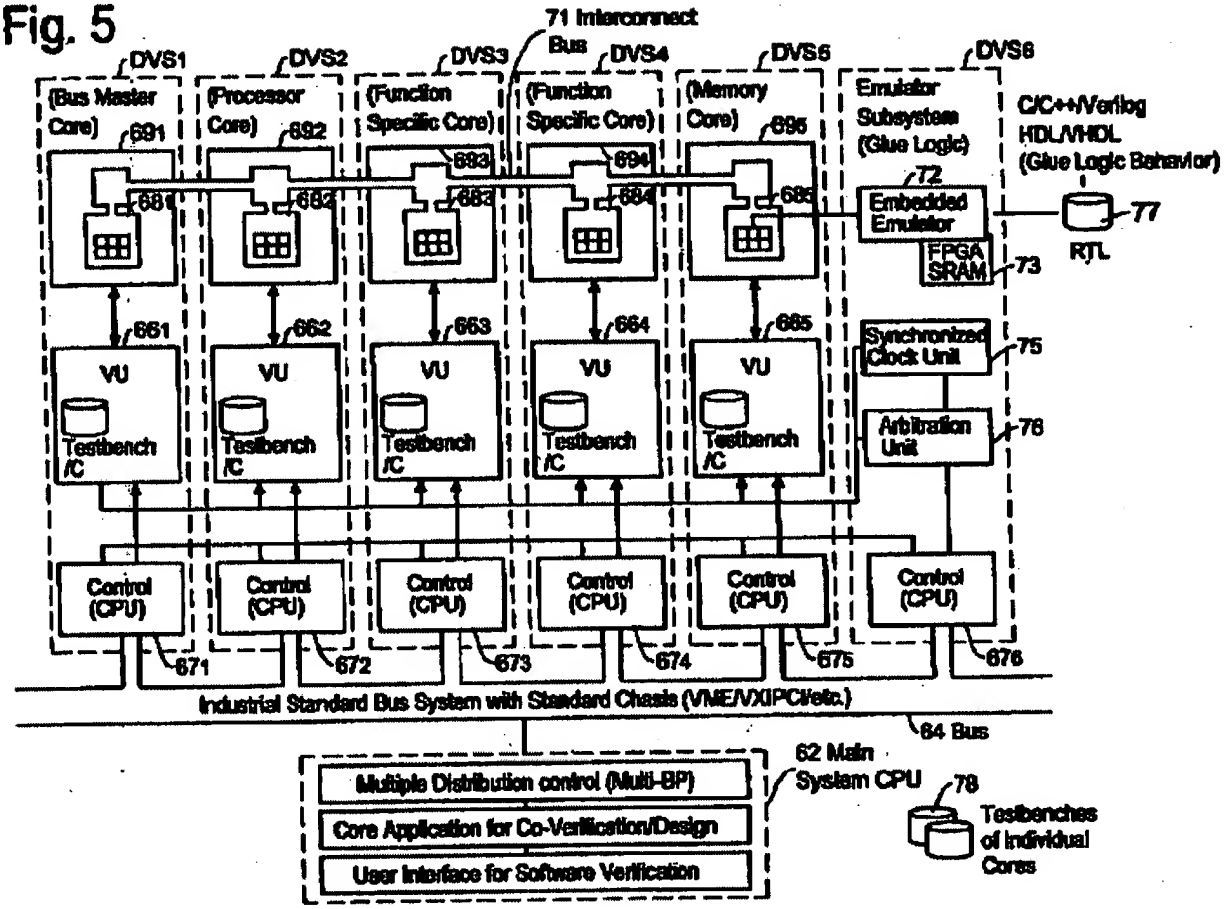
> FIG. 7 shows the emulator sub-system. In this approach, any commercial emulator system can be used. In FIG. 7, the emulator 72 is loaded with the synthesizable RTL of glue logic and with the testbench data in the glue logic testbench file 77. The synchronization unit and arbitration units are used with commercial emulator to interface it with other VUs 66. The control CPU 67 performs the synchronization and communication tasks with the main system CPU 62.

The citation of Column 10 shows that there is data flow between the VU's, specifically **"data flow at a design validation station level (from one VU to another)"**. Column 11 further indicates that synchronization and arbitration of the VU's is performed by the control CPU and main system CPU. The reference teaches synchronization and arbitration of the VU's as well as data flow between the VU's. In addition Column 13, Lines 5-15 of the reference states:

> FIG. 11 shows a further example of design validation station of the present invention wherein a plurality of verification units (VU) are directly controlled by the main system computer. In this example, unlike the previous examples, each design validation station does not include control CPU but directly controlled by the main system computer 62 through the system bus 64. Thus, all tasks such as synchronization, response evaluation of cores, timing evaluation, and overall SoC evaluation, etc., are carried out by the main system computer 62.

This citation shows that the CPU deals with tasks such as synchronization, etc when evaluating the overall SoC. Since the VU's are connected to each other as well as the CPU they therefore posses a shared memory in which tasks such as synchronization and overall evaluation must be carried out by utilizing multiple VU's. This is further reinforced in Figure 5 for example where the overall SoC evaluation must evaluate a memory, function, bus, processor, etc. in conjunction therefore the arbitration, synchronization, and overall evaluation utilizes multiple VU'S connected together via the CPU and provided data to each other via the CPU for purposes of arbitration, synchronization, and/or overall evaluation. This is further seen in Figure 5 of the reference reproduced below:

Fig. 5



The Main System CPU, element 62 is connected to the Control CPU's, elements 671-676, which are further connected to the Arbitration unit, element 76, as well as the Synchronized clock unit, element 75 which are further connected to the VU's, elements 661-665. Since the Main CPU carries out synchronization, response evaluation of cores, timing evaluation, and **overall SoC evaluation**, etc. the Main CPU possesses the shared data memory to allow for complete evaluation of the SoC.

(10.2) Appellant argues that the reference does not disclose independently of advancement of simulated time.

Examiners Answer:

First, the Examiner would like to note that Appellants appear to be reading limitations into the claims that are neither supported by the specification nor explicitly stated by the claims. Specifically, the aspect of "zero system time" which is neither recited in the claims nor in the specification of the instant application.

However, As previously stated by the Examiner, Column 12, Lines 15-52 of the reference states:

To achieve this, the main system CPU **62** contains a multiple distribution control with multiple bus protocol (shown as multi-BP in FIGS. **5** and **9**). It performs a "Fork" operation on the application task (software application) to break it into multiple sub-tasks, schedule them and assign these sub-tasks to different VUs **66** that are mapped to individual cores. It should be noted that this "Fork" operation is performed on the application software that is in a high level language such as Verilog/VHDL or even C/C++ language. Thus, the system compiler with multiple distribution control can perform "Fork" on the application task to execute it in a distributed computing environment made up of the multiple verification units **66**.

After this "Fork" operation, the sub-tasks are distributed to individual VUs **66** through the system bus **64**. The control CPU **67**, arbitration unit **76** and synchronization clock unit **75** allow the communication and error-free data transfer from the main system CPU **62** to control CPUs **67** of the individual VUs **66**. This architecture with the main system CPU **62**, arbitration unit **76** and synchronization clock unit **75** is shown in FIG. **9**.

Based upon the sub-task assignments, the control CPUs **67** apply event-based vectors to the individual cores and collect response therefrom. This response is passed to the main system CPU **62**, again using the control CPU, bus arbitration poll unit and synchronization unit for error-free data transfer. The main system CPU **62** performs a "Join" operation to merge various responses and to form an SoC level response. This response is compared with the simulation response to determine if SoC performed correct operation. If this is an application run, then this response is the expected outcome of the application. For example a video application run should result in display of a picture frame. Any deviation from the simulation data or expected application output is identified by the main system CPU **62** and easily debugged by the design engineer because the environment is event based that is the same as the original design environment.

This section indicates that different parts of the SoC are executed at different times, which requires time defining events that either advance or slow down the execution of an event. Further, Figure 5 element 75 is a synchronization clock unit, which synchronizes the multiple VU's in order to determine overall SoC evaluation. These two sections are exemplary of the type of time defining events performed by the reference and anticipate Appellants' claimed limitation.

Appellants seem to argue that the references' buses will take longer to enable communication than the shared data memory disclosed in the claims however the Examiner is puzzled by this assertion since as per paragraphs 35 and 39 of the specification of the instant application, Appellants claimed XVC's (External Verification Controllers) are also connected via a bus.

> **[0035] FIG. 2** schematically illustrates a more complex system that is being simulated, validated and tested. In this example, a large number of XVCs are provided each associated with different hardware blocks within the hardware being simulated. The hardware being simulated contains a microprocessor core. Due to the complexity and speed difficulties in simulating the actions of a microprocessor core, this embodiment instead reads pre-generated test vectors simulating the interaction of the microprocessor core with the other elements of the model and applies these test vectors to the appropriate bus such that the other elements within the hardware simulation can respond to those test vectors as if they had been generated by the processor core.

> **[0039] FIG. 5** schematically illustrates the information flow between some of these separate processors. It will be seen that the XVC applies stimulus to and receives responses from the hardware simulation. The hardware simulation itself interacts with other elements within the hardware simulation via a bus interface. The XTSM exchanges test scenario controlling messages with the XVC including messages that trigger an event, stop an event and return a read value from the scoreboard (shared data memory). The XVC can generate its own test scenario controlling messages that are passed back to the XTSM and onto other XVCs indicating that a particular XVC event has occurred. The XVC may also request to write a value to the scoreboard or to read a value from the scoreboard. The score board provides an appropriate mechanism for XVCs sharing data and for the reporting of diagnostic information from an

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the Examiner in the Related Appeals and Interferences section of this Examiner's Answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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